

BiCS5 TLC/aSLC Flash

(3D NANA TLC BiCS5)

M.2 SATA III Module

PHANES-W Series

M.2 2242/2280 Type

Document No. : 100-xBMDS-PWCT5xBM

Version No. : 02V1

Date: September. 2025

ISO 9001 : 2015 CERTIFIED



Product Features

■ Flash IC

- 3D-NAND TLC Flash BiCS5 Flash.

■ Compatibility

- Compliant with SATA Revision 3.1
- SATA 1.5Gbps/3.0Gbps/6.0Gbps data transfer rate.
- ATA-8 ACS3 command set

■ Additional Capabilities

- S.M.A.R.T.*¹ (Self-Monitoring, Analysis and Reporting Technology) feature set support.
- Thermal Monitor for SSD's temperature.
- Native Command Queuing (NCQ) support.
- TRIM maintenance command support.
- Both Static & Dynamic wear-leveling algorithm
- Hardware Low Density Parity Check Code, LDPC support.
- Support Over-Provisioning.
- Support expands register for SATA protocol 48 bits addressing mode.
- Support DIPM/HIPM Mode.

■ Mechanical

- Interface compatible with PCI Express™ M.2 2280)
- M.2 keying notches in B and M positions.
- **Dimension:**
2242: 42 mm x 22 mm.
2280: 80 mm x 22 mm.
- **Weight:**
2242: 5.00 g / 0.28 oz.
2280: 8.00 g / 0.176 oz.

■ Power Operating Voltage 3.3V(+/-) 5%

- Active Read (Max.) ≤ 1,750 mW. (2TB)
- Active Write (Max.) ≤ 1,450 mW. (2TB)
- Idle < 210 mW. (2TB)

■ Performance (Maximum value) *²

- **Sequential Read:** up to 550 MB/s (2TB)
- **Sequential Write:** up to 510 MB/s (2TB)
- **Random 4K Read:** up to 93.5K IOPS (2TB)
- **Random 4K Write:** up to 85.0K IOPS (2TB)

■ Capacity

- **2242:** 3D: 64GB~1TB. / 3D aSLC:16GB~256GB
- **2280:** 3D: 128GB~2TB. / 3D aSLC:32GB~512GB

■ Reliability

- **TBW:** Up to 2,900 TBW at 2TB Capacity.
(Client workload by JESD-219A)
- **ECC:** Designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding.
- **MTBF:** <3 million hours.
- **UBER:** < 1 sector per 10¹⁶ bits.
- **Temperature:** (Operating)
Standard Grade: 0°C ~ +70°C
Wide Temp. Grade: -40°C ~ +85°C
- **Vibration:** 80 Hz to 2000 Hz, 20G, 3 axes
- **Shock:** 0.5ms, 1500 G, 3 axes

■ Certifications and Declarations

- **Certifications:** CE & FCC
- **Declarations:** RoHS & REACH

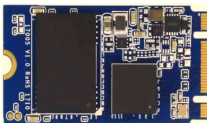
Remarks:

1. Support official S.M.A.R.T. Utility.
2. Sequential performance is based on CrystalDiskMark 6.0.0 with file size 1000MB
3. **BiCS** means Bit Cost Scalable Technology.

BiCS FLASH is a trademark of KIOXIA Corporation.

Order Information

◆ APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series – 2242 Form-factor

Product Picture	Grade	Standard grade (0°C ~ 70°C)	Wide Temp. Grade (40°C ~ +85°C)
	Kioxia BiCS5 TLC		
	64GB	SBMDS064G-PWCT54BM	WBMDS064G-PWIT54BM-C
	128GB	SBMDS128G-PWCT54BM	WBMDS128G-PWIT54BM-C
	256GB	SBMDS256G-PWCT54BM	WBMDS256G-PWIT54BM-C
	512GB	SBMDS512G-PWCT54BM	WBMDS512G-PWIT54BM-C
	1TB	SBMDS001T-PWCT54BM	WBMDS001T-PWIT54BM-C
	Kioxia BiCS5 aSLC		
	16GB	SBMDS016G-PWCT54BM	WBMDS016G-PWIT54BMAS
	32GB	SBMDS032G-PWCT54BM	WBMDS032G-PWIT54BMAS
	64GB	SBMDS064G-PWCT54BM	WBMDS064G-PWIT54BMAS
	128GB	SBMDS128G-PWCT54BM	WBMDS128G-PWIT54BMAS
	256GB	SBMDS256G-PWCT54BM	WBMDS256G-PWIT54BMAS

◆ APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series – 2280 Form-factor

Product Picture	Grade	Standard grade (0°C ~ 70°C)	Wide Temp. Grade (40°C ~ +85°C)
	Kioxia BiCS5 TLC		
	128GB	SBMDS128G-PWCT58BM	WBMDS128G-PWIT58BM-C
	256GB	SBMDS256G-PWCT58BM	WBMDS256G-PWIT58BM-C
	512GB	SBMDS512G-PWCT58BM	WBMDS512G-PWIT58BM-C
	1TB	SBMDS001T-PWCT58BM	WBMDS001T-PWIT58BM-C
	2TB	SBMDS002T-PWCT58BM	WBMDS002T-PWIT58BM-C
	Kioxia BiCS5 aSLC		
	32GB	SBMDS032G-PWCT58BM	WBMDS032G-PWIT58BMAS
	64GB	SBMDS064G-PWCT58BM	WBMDS064G-PWIT58BMAS
	128GB	SBMDS128G-PWCT58BM	WBMDS128G-PWIT58BMAS
	256GB	SBMDS256G-PWCT58BM	WBMDS256G-PWIT58BMAS
	512GB	SBMDS512G-PWCT58BM	WBMDS512G-PWIT58BMAS

I. Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 — **X11 X12 X13 X14 X15 X16 X17 X18** — **X20**

X1 : Grade

S: Standard Grade – operating temp. 0° C ~ 70 ° C

W: Wide Temp. Grade – operating temp. -40° C ~ +85 ° C

X13 : Controller Grade

C : Commercial grade

I : Industrial grade

X2 : The material of case

B : Bare PCBA w/o Casing

X14 X15 : Flash IC

T5 : 3D-NAND TLC Flash BiCS5 Flash

X3 X4 X5 : Product category

MDS : M.2 SATA III host interface

X16 X17 X18 : Form-Factor

4: 2242 Type

8: 2280 Type

BM: with two notches in B and M positions use up to two PCI Express lanes and provide broader compatibility at the same time

X6 X7 X8 X9 : Capacity

016G: 16GB **256G** 256GB

032G: 32GB **512G:** 512GB

064G: 64GB **001T:** 1TB

128G: 128GB **002T:** 2TB

X19 X20 : Reserved for specific requirement

C : Conformal-coating (optional)

AS : aSLC mode

X11 : Controller

P : PHANES Series

X12 : Controller version

A, B, C.....W

Revision History

Revision	Description	Date
1.0	Initial release.	2024/05/17
2.0	Add. 2242 form-factor	2024/08/13
2.1	Update Secure Erase Add. aSLC solution.	2025/09/04

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1. Introduction

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provides high-capacity flash memory Solid State Drive (SSD) that electrically complies with SATA Revision 3.1 standard.

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series, it supports SATA 1.5Gbps/3.0Gbps/6.0Gbps data transfer rate with high performance. There are 2242 & 2280 form-factor available. The operating temperature grade is optional for Standard grade 0°C ~ 70°C and wide temp grade supports -40°C ~ +85°C.

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provide the ultra-high speed for embedded or server operations with space constraints for host computing systems; the data transfer performance by sequential read is up to 550.0 MB/sec, and sequential write is up to 510.0 MB/sec. which is based on BiCS5 BiCS5 TLC/aSLC flash.

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series PCB design with two notches in B and M positions use up to two PCI Express lanes and provide broader compatibility at the same time for M/B socket mounting, while the M.2 modules with only one notch in the M position use up to four PCI Express lanes; both examples we provide APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series to be a SATA storage devices.

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provide a high-level interface to the host computer. This interface allows a host computer to issue commands to the APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series to read or write blocks of memory. A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

Figure1 Shows a block diagram of APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series.

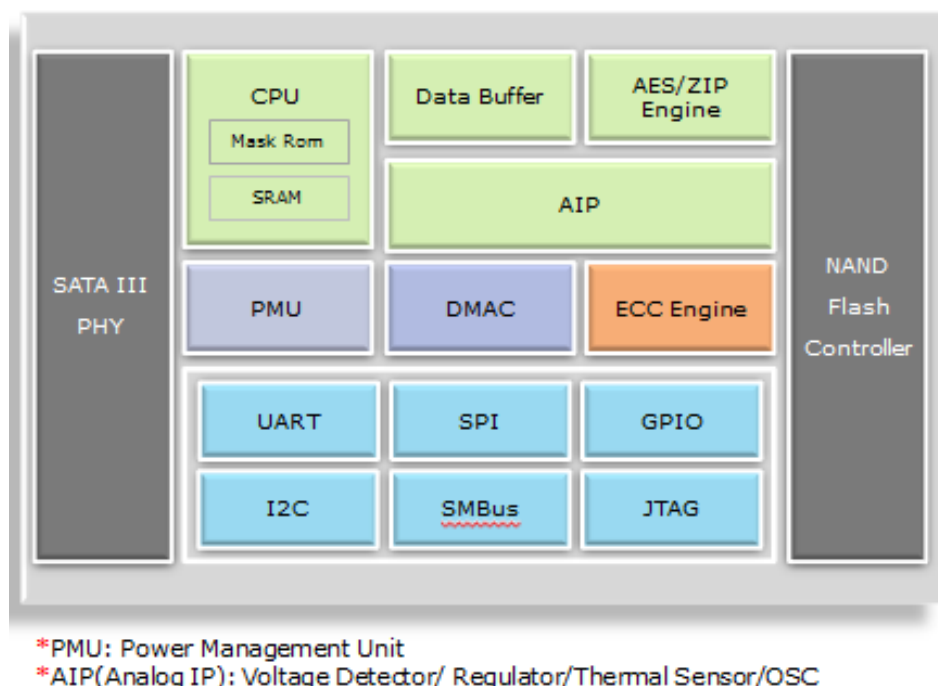


Figure 1: APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series block diagram

1.1. Scope

This document describes features, specifications and installation guide of APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. Flash Management Technology - Static & Dynamic Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3. Bad Block Management

➤ Early Bad Block

The fault block generated during the manufacturing process of NAND Flash is called Early Bad Block.

➤ Later Bad Block

In the process of use, as the number of operations of writing and erasing increases, a fault block is gradually generated, which is called a Later Bad Block.

Bad block management is a management mechanism for a bad block to be detected by the control IC and mark bad blocks in the NAND Flash and improve the reliability of data access. The bad block management mechanism of the control IC will establish a **Bad Block Table** when the NAND Flash is started for the first time, and will also record the errors found in the process of use in the bad block table, and data is ported to new valid blocks to avoid data loss.

In order to detect the initial bad blocks to handle run time bad blocks, APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provides the **Bad Block Management** scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

1.4. Error Correcting Coding (ECC)

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series to read or write blocks of memory.

A powerful hardware design is architecture multiplied LDPC (Low Density Parity Check) for Error Correcting Coding (ECC). APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, bad block management and diagnostics, power management and clock control.

1.5. 3D-NAND Flash

3D NAND is a vertical implementation of the NAND flash cell memory array. The memory cell transistors forming the NAND string are connected in a series vertically and the memory transistors are changed from the floating-gate type to a trapped charge type.

In floating-gate technology, die density is increased by shrinking peripheral circuits and active circuits.

With 3D, holding the X/Y dimension of the die constant, die density is increased through multiple layers of the active circuits on the Z axis. Higher-density 3D NAND die enables applications needing high-density NAND chip solutions.

1.6. Over-Provisioning

Over-Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users.

With Over-Provisioning, the performance and IOPS (Input / Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.7. Thermal Monitor

Thermal monitors are devices for measuring temperature, and can be found in SSDs in order to issue warnings when SSDs go beyond a certain temperature. The higher temperature the thermal monitor detects, the more power the SSD consumes, causing the SSD to get aging quickly. Hence, the processing speed of a SSD should be under control to prevent temperature from exceeding a certain range. Meanwhile, the SSD can achieve power savings.

1.8. Low Power Management

1.8.1. DEVSLP Mode (Optional)

With the increasing need of aggressive power/battery life, SATA interfaces include a new feature, Device Sleep (DEVSLP) mode, which helps further reduce the power consumption of the device. DEVSLP enables the device to completely power down the device PHY and other sub-systems, making the device reach a new level of lower power operation. The DEVSLP does not specify the exact power level a device can achieve in the DEVSLP mode, but the power usage can be dropped down to 5mW or less.

1.8.2. DIPM/HIPM Mode

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. For Partial mode, the device must resume to full operation within 10 microseconds, whereas the device will spend 10 milliseconds to become fully operational in the Slumber mode. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

1.9. Secure Erase

Secure Erase is a standard ATA command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

1.10. UBER

Table 1: UBER Calculation.

Capacity	UBER
16GB ~ 2TB	< 1 sector per 10 ¹⁶ bits read

Notes:

- UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
- $UBER = FER \text{ (fail rate)} / \text{Data Size (user data bit)}$
- $FER = \text{uncorrectable ECC frame number} / \text{total ECC frame number}$
- 4. LDPC for Kioxia 3D ECC capability > 120bit/KB.

1.11. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Table 2: MTBF Calculation.

Capacity	MTBF
16GB ~ 2TB	> 3 million hours

1.12. SSD Lifetime Management Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device.

To calculate the TBW of a SSD, the following equation is applied:

$$TBW = [(NAND \text{ Endurance}) \times (SSD \text{ Capacity}) / WAF]$$

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 3: Environmental Specification

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series		Standard Grade	Wide Temp Grade
Temperature	Operating:	0°C ~ +70°C	-40°C ~ +85°C
	Non-operating:	-40°C ~ +85°C	-40°C ~ +85°C
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Frequency/Acceleration:	80 Hz to 2000 Hz, 20G, 3 axes	
Shock	Operating & Non-operating:	0.5ms, 1500 G, 3 axes	
Electrostatic Discharge (ESD)	Temperature:	24°C	
	Relative Humidity:	49% (RH)	
	+/-4KV:	Device functions are affected, but EUT will be back to its normal or operational state automatically.	

2.2. System Power Requirements

Table 4: Power Requirement

Operating Voltage: 3.3V, +/- 5% (3.14 ~ 3.46V) Unit: mW							
Flash Type	Capacity	Flash Structure	Read	Write	Partial	Slumber	Idle
BiCS5 TLC	64GB	64GB x 1, BiCS5 TLC, BGA	850	750	65	25	180
	128GB	128GB x 1, BiCS5 TLC, BGA	1,050	1,100	75	35	190
	256GB	256GB x 1, BiCS5 TLC, BGA	1,150	1,350	75	35	190
	512GB	256GB x 2, BiCS5 TLC, BGA	1,150	1,350	75	35	190
	1TB	512GB x 2, BiCS5 TLC, BGA	1,200	1,400	75	40	195
	2TB	512GB x 4, BiCS5 TLC, BGA	1,450	1,750	65	27	210
BiCS5 aSLC	16GB	64GB x 1, BiCS5 aSLC, BGA	820	750	65	25	175
	32GB	128GB x 1, BiCS5 aSLC, BGA	1,150	1,150	65	25	175
	64GB	256GB x 1, BiCS5 aSLC, BGA	1,150	1,150	65	25	175
	128GB	256GB x 2, BiCS5 aSLC, BGA	1,250	1,200	65	25	175
	256GB	512GB x 2, BiCS5 aSLC, BGA	1,320	1,200	65	25	175

Notes:

- The average value of power consumption is achieved based on 100% conversion efficiency.
- Samples were built using Kioxia BiCS5 3D-TLC NAND Flash.
- Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CrystalDiskMark.
- Power Consumption may differ according to flash configuration, SDR configuration, or platform.
- Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH.

2.3. System Performance

Table 5: System Performances

Flash Type	Capacity	Flash Structure	Sequential (MB/s)		4K Random (IOPS)	
			Read	Write	Read	Write
BiCS5 TLC	64GB	64GB x 1, BiCS5 TLC, BGA	380	265	36,500	57,500
	128GB	128GB x 1, BiCS5 TLC, BGA	550	450	44,500	78,500
	256GB	256GB x 1, BiCS5 TLC, BGA	550	485	75,500	82,500
	512GB	256GB x 2, BiCS5 TLC, BGA	550	500	91,500	83,500
	1TB	512GB x 2, BiCS5 TLC, BGA	550	500	96,000	85,500
	2TB	512GB x 4, BiCS5 TLC, BGA	550	510	96,000	85,500
BiCS5 aSLC	16GB	64GB x 1, BiCS5 aSLC, BGA	335	270	25,000	55,000
	32GB	128GB x 1, BiCS5 aSLC, BGA	540	460	49,000	77,500
	64GB	256GB x 1, BiCS5 aSLC, BGA	540	485	85,500	82,000
	128GB	256GB x 2, BiCS5 aSLC, BGA	545	500	93,500	83,000
	256GB	512GB x 2, BiCS5 aSLC, BGA	545	500	93,500	83,000

Note:

- Performance may differ according to flash configuration, use condition, environment and platform.
- Use CrystalDiskMark 6.0.0 with Q32T1, 1GB range for sequential read/write test.
- Performance specification is under that Thermal Throttling has not worked yet.
- Operating System: Windows 10 Professional (x64)
- Intel Core i7-8700K CPU @ 3.70GHz
- Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

2.4. System Reliability

Table 6: System Reliability

Wear-leveling Algorithms		Static and Dynamic wear-leveling algorithms			
Bad Block Management		Supportive			
ECC Technology		Hardware design LDPC (Low Density Parity Check)			
Erase counts		KIOXIA BiCS5 TLC : 3K P/E Cycles / BiCS5 aSLC : 30K P/E Cycles			
		BiCS5 TLC		BiCS5 aSLC	
		TBW	DWPD	TBW	DWPD
Capacity	16GB	N/A	N/A	430	24.54
	32GB	N/A	N/A	1,000	28.53
	64GB	65	0.92	3,000	42.81
	128GB	90	0.64	6,400	45.66
	256GB	220	0.78	13,000	46.37
	512GB	540	0.96	N/A	N/A
	1TB	1,200	1.07	N/A	N/A
	2TB	2,900	1.29	N/A	N/A

Note:

- TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3,000. It may differ according to flash configuration and platform configuration.
- DWPD (Drive Write Per Day) is calculated based on 3-year lifetime.
- $DWPD = TBW / (365 \text{ days} \times 3 \text{ years} \times \text{User Capacity})$
- The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

2.5. Device Capacity

Table 7: User Capacity and Addressable Sectors

Capacity	Number of Total LBA		User Available Bytes
	512Bytes/Sector	4KBytes/Sector	
16GB	31,277,232	3,909,654	16,013,942,784
32GB	62,533,296	7,816,662	32,017,047,552
64GB	125,045,424	15,630,678	64,023,257,088
128GB	250,069,680	31,258,710	128,035,676,160
256GB	500,118,192	62,514,774	256,060,514,304
512GB	1,000,215,216	125,026,902	512,110,190,592
1TB	2,000,409,264	250,051,158	1,024,209,543,168
2TB	4,000,797,360	500,099,670	2,048,408,248,320

Note:

- 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
- The calculation is following IDEMA Standard.
- The total actual user usable capacity of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.
- Eg : OS shows 119.24GB (NTFS) with 128GB SSD device.

2.6. Physical Specifications

Refer to Table 5 and see Figure 2 for APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series physical specifications and dimensions.

Table 8: Physical Specifications of APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series

Form-Factor	Length:	Width:	Weight:
2242	42.0 (± 0.15) mm	22.0 (± 0.15)	5.00 g / 0.17 oz.
2280	80.0 (± 0.15) mm	22.0 (± 0.15)	8.00 g / 0.28 oz.

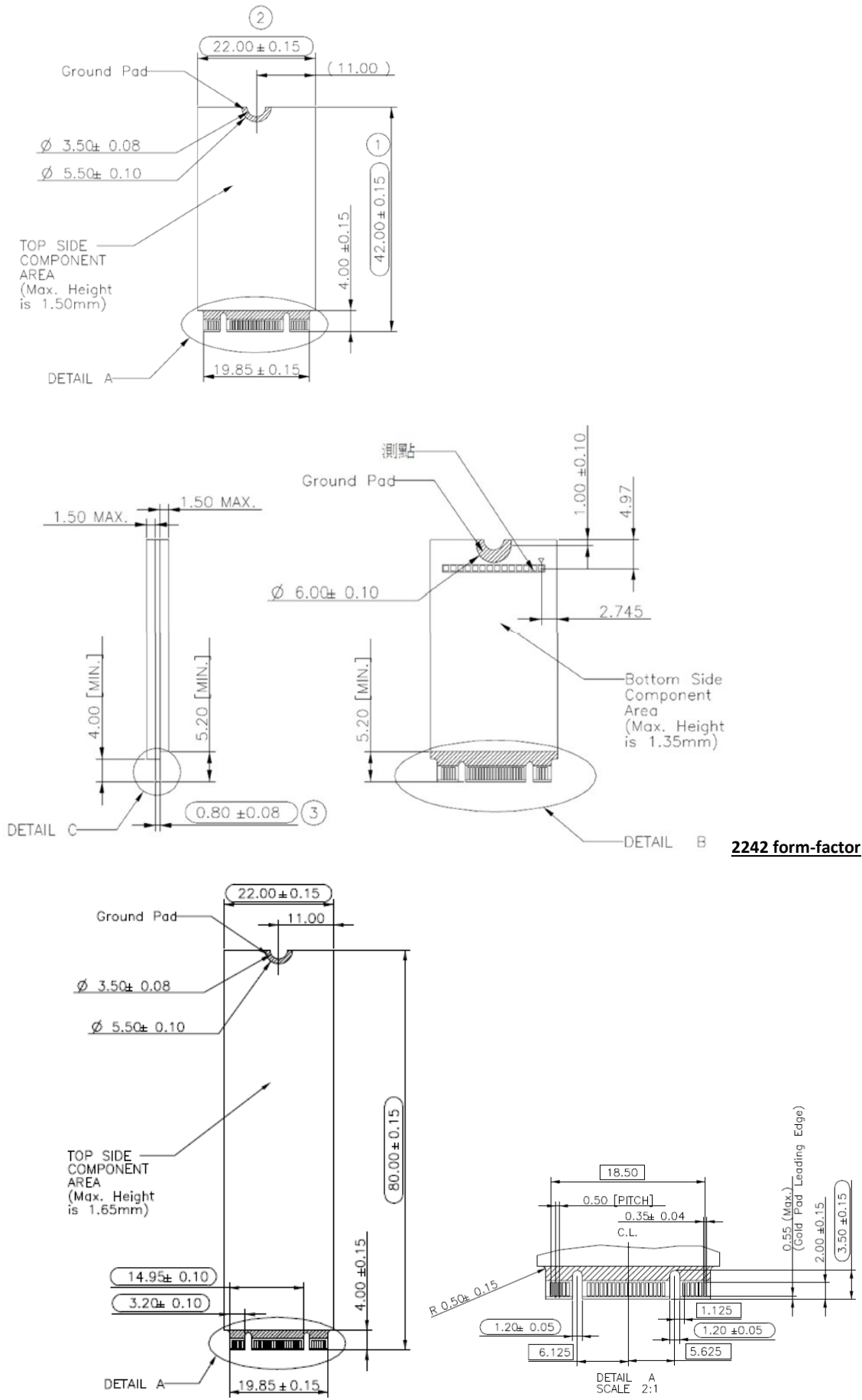


Figure 3: APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series – 2242/ 2280 Dimension

2.7. B+M Key M.2 SSD Assembly Precautions

B+M Key M.2 SSD (Figure1 below) is compatible to both B Key (Figure2) and M Key (Figure3) sockets. However, B-Key notch is not identical to M-Key notch so user should distinguish the mating keys first and then slide M.2 SSD into the sockets accordingly. Misuse may cause severe damages to SSD including burn-out.

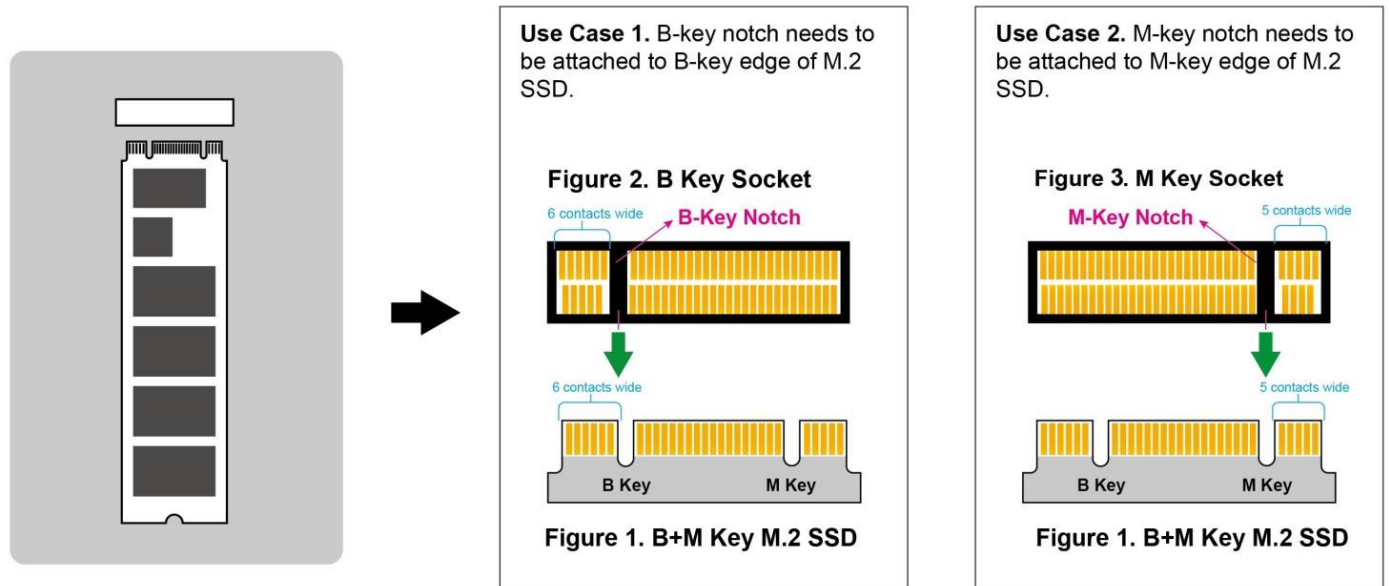


Figure 4: B+M Key M.2 Assembly Precautions

3. Interface Description

3.1. M.2 SATA III Module interface

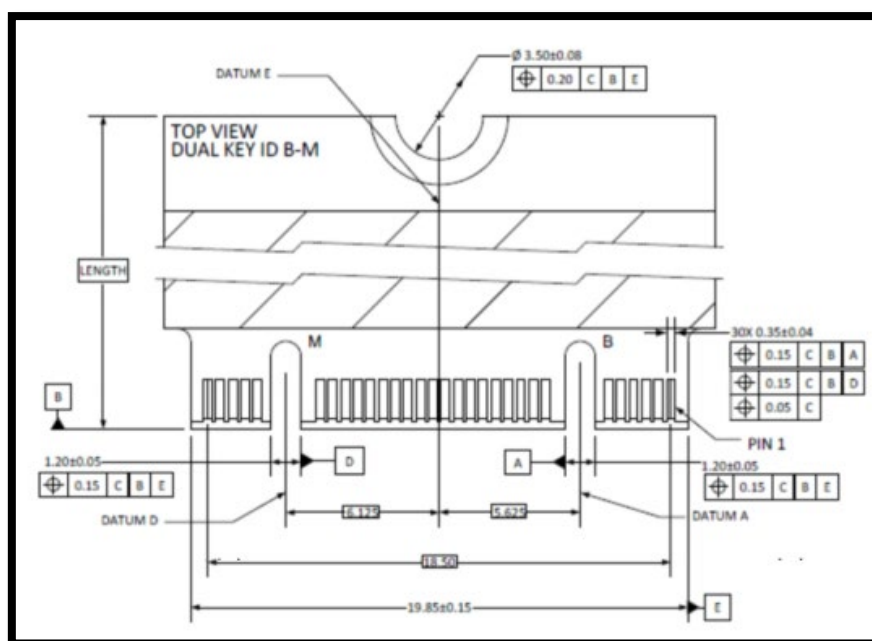


Figure 5: The connectors of Signal Segment and Power Segment

3.2. Pin Assignments

APRO BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series operates with standard SATA pin-out. The pin assignments are listed in below table 6.

Table 9 - Pin Assignments

Pin #	SATA Pin	Description
1	CONFIG_3 = GND	Ground
2	3.3V	Supply pin
3	GND	Ground
4	3.3V	Supply pin
5	N/C	No Connect
6	N/C	No Connect
7	N/C	No Connect
8	N/C	No Connect
9	N/C or GND Note	No Connect or Ground
10	DAS/DSS# (O) (OD)	Status indicators via LED devices that will be provided by the system Active Low. A pulled-up LED with series current limiting resistor should allow for 9mA when On.
11	N/C	No Connect
12	Module Key	
13	Module Key	
14	Module Key	
15	Module Key	
16	Module Key	
17	Module Key	
18	Module Key	
19	Module Key	
20	N/C	No Connect
21	CONFIG_0 = GND	Ground
22	N/C	No Connect
23	N/C	No Connect
24	N/C	No Connect
25	N/C	No Connect
26	N/C	No Connect
27	GND	Ground
28	N/C	No Connect
29	N/C	No Connect
30	N/C	No Connect
31	N/C	No Connect
32	N/C	No Connect

33	GND	Ground
34	N/C	No Connect
35	N/C	No Connect
36	N/C	No Connect
37	N/C	No Connect
38	DEVSLP (I) (0/3.3V) (Optional)	Device Sleep, Input. When driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	N/C	No Connect
41	SATA-B+	SATA differential signals in the SATA specification
42	N/C	No Connect
43	SATA-B-	SATA differential signals in the SATA specification
44	N/C	No Connect
45	GND	Ground
46	N/C	No Connect
47	SATA-A-	SATA differential signals in the SATA specification
48	N/C	No Connect
49	SATA-A+	SATA differential signals in the SATA specification
50	N/C	No Connect
51	GND	Ground
52	N/C	No Connect
53	N/C	No Connect
54	N/C	No Connect
55	N/C	No Connect
56	Reserved for MFG Data	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG Clock	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket
59	Module Key	
60	Module Key	
61	Module Key	
62	Module Key	
63	Module Key	
64	Module Key	
65	Module Key	
66	Module Key	
67	N/C	No Connect

68	SUSCLK (I) (0/3.3V)	No Connect
69	CONFIG_1 = GND	Defines module type
70	3.3V	Supply pin
71	GND	Ground
72	3.3V	Supply pin
73	GND	Ground
74	3.3V	Supply pin
75	CONFIG_2 = GND	Ground

Note:

- N/C for Socket 2, and GND for Socket 3.
- No support low power mode.

Appendix A: Limited Warranty

APRO warrants your BiCS5 TLC/aSLC M.2 SATA III SSD PHANES-W Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

WARRANTY PERIOD:

- **BiCS5 TLC (Standard grade / Wide Temp. grade) 2 years / Within 3K Erasing Counts**
- **BiCS5 aSLC (Standard grade / Wide Temp. grade) 2 years / Within 30K Erasing Counts**

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